

# RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. FIRST SEMESTER EXAMINATION, DECEMBER 2019

FIRST YEAR [BATCH 2019-22]

COMPUTER SCIENCE (General)

Date : 16/12/2019

Time : 11 am – 1 pm

Paper : I

Full Marks : 50

Answer **any five** questions of the following:

[5×10]

1. a) Reduce the following expression using K-map:  $f = \sum m(2, 3, 6, 7, 8, 10, 11, 13, 14)$ .  
b) Implement the following Boolean function with a multiplexer  
 $F(A, B, C, D) = \sum(1, 2, 5, 8, 12, 15)$ .  
c) State De Morgan's Theorem. (4+4+2)
2. a) Find the dual and complement of the following expression:  $f = \left[ (\overline{ab})a \right] \left[ (\overline{ab})b \right]$ .  
b) Implement full subtractor using logic gates only.  
c) What is a code converter? ((2+2)+5+1)
3. a) Expand  $A + \overline{BC} + \overline{ABD} + ABCD$  to maxterms.  
b) Design a combinational circuit with three inputs and one output. The output is equal to 1 when the binary value of the input is less than 3. The output is 0 otherwise.  
c) What is ripple carry adder? (4+5+1)
4. a) Apply De Morgan's theorem to the expression  $f = \overline{AB(C\overline{D} + \overline{E}F)}(\overline{AB} + CD)$ .  
b) Explain internal structure of a hard disk drive with suitable diagram.  
c) What do you mean by Universal Gates? (3+5+2)
5. a) Draw and explain circuit diagram of a BCD adder.  
b) Find out the relationship between numbers of redundant bits (r) required to correct d data bits with respect to Hamming Code. (6+4)
6. a) Explain the functioning of an odd parity generators and checker with suitable example.  
b) Draw a 4-bit universal shift register with parallel load. (5+5)
7. a) Perform the following base conversions:  
i)  $(100011.011)_2 = (?)_{10}$   
ii)  $(A2.6F)_{16} = (?)_8$   
b) What is the drawback of D-flipflop? How it can be resolved?  
c) How floating point number is represented in memory? ((2.5+2.5)+3+2)
8. a) Differentiate between the followings:  
i) SRAM and DRAM  
ii) Compiler and Interpreter  
b) Design a BCD to Excess-3 code converter. ((2+2)+6)

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